CMOS current-controlled current differencing transconductance amplifier and applications to analog signal processing

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Abstract

This article presents design of a basic current-mode building block for analog signal processing, named as current-controlled current differencing transconductance amplifier (CCCDTA). Its parasitic resistances at two current input ports can be controlled by an input bias current. Owing to working in current-mode of all terminals, it is very suitable to use in a current-mode signal processing, which is continually more popular than a voltage one. The proposed element is realized in a CMOS technology and is examined the performance through PSPICE simulations. They display usability of the new active element, where the maximum bandwidth is 311 MHz. The CMOS CCCDTA performs low power consumption and tuning over a wide current range. In addition, some examples as a current-mode universal biquad filter, floating inductance simulator and quadrature oscillator are included. They occupy only single CCCDTA.

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1. Introduction

In the last decade, there has been much effort to reduce the supply voltage of electronic circuits. This is due to the command for portable and battery-powered equipment. Since a low-voltage operating circuit becomes necessary, the current-mode technique is ideally suited for this purpose more than the voltage-mode one. Consequently, there is a growing interest in synthesizing the current-mode circuits because of more their potential advantages such as larger dynamic range, higher signal bandwidth, greater linearity, simpler circuitry and low power consumption [1,2]. Many active elements able to function in current-mode such as OTA, current conveyor and current differencing buffered amplifier (CDBA), have been introduced to respond these demands.

Recently, a reported 5-terminals active element, namely current differencing transconductance amplifier (CDTA) [3], seems to be a versatile component in the realization of a class of analog signal-processing circuits, especially analog frequency filters [4,5]. It is really current-mode element whose input and output signals are currents. It should also be noted here that, the CDTA offers wider frequency bandwidth advantages as compared to its close relative, the CDBA [6]. In addition, it can also be adjusted the output current gain. However, from our investigations, there are seen that the CDTA cannot be controlled the parasitic resistances at two current input ports so when it used in some circuits, it must unavoidably require some external passive components.
especially the resistors. This makes it not appropriate for IC implementation due to occupying more chip area.

The purpose of this paper is to design and synthesize a modified-version CDTA, which is newly named current controlled current differencing transconductance amplifier (CCCDTA) and using a CMOS technology. The parasitic resistances at two current input ports can be controlled by an input bias current, then it does not need a resistor in practical applications. The performances of proposed CCCDTA are illustrated by PSPICE simulations, they show good agreement as mentioned. Some example applications as a universal filter, floating inductance simulator and quadrature oscillator are comprised.

2. Circuit configuration

2.1. Basic concept of CCCDTA

CCCDTA properties are similar to the conventional CDTA, except that input voltages of CCCDTA are not zero and the CCCDTA has finite input resistances \( R_p \) and \( R_n \) at the p and n input terminals, respectively. These parasitic resistances are equal and can be controlled by the bias current \( I_{B1} \) as shown in the following:

\[
\begin{bmatrix}
V_p \\
V_n \\
I_p \\
I_n \\
I_c
\end{bmatrix} =
\begin{bmatrix}
R_p & 0 & 0 & 0 & 0 \\
0 & R_n & 0 & 0 & 0 \\
1 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & \pm g_m & 0 \\
0 & 0 & 0 & 0 & \pm \frac{g_m}{g_m}
\end{bmatrix}
\begin{bmatrix}
I_p \\
I_n \\
I_c \\
V_x \\
V_z
\end{bmatrix},
\]  

(1)

The symbol and the equivalent circuit of the CCCDTA are illustrated in Fig. 1(a) and (b), respectively.

2.2. A current differencing circuit which has finite input resistances

Fig. 2 displays a class AB translinear loop, which is used as input section. By straightforward analysis, we will obtain the parasitic resistance at input terminal as

\[
R_{in} = \frac{1}{g_{m2} + g_{m5}} - \frac{I_{B1}}{I_{in}(g_{m2} + g_{m5})} \left(\frac{g_{m2}}{g_{m1}} - \frac{g_{m5}}{g_m}\right).
\]  

(2)

From Eq. (2) if \( g_{m1} = g_{m4} \) and \( g_{m2} = g_{m5} = g_m \), we will obtain

\[
R_{in} = \frac{1}{2g_m} = \frac{1}{\sqrt{\beta_n I_{B1}}},
\]  

(3)

where \( \beta_n = \mu_n C_{ox} (W/L) \) is the physical parameter of MOS transistor. Based on the use of the finite input resistance input stage of Fig. 2, the unity gain current amplifier can be shown in Fig. 3. From routine circuit analysis, the output current \( I_O \) of this circuit can be expressed as

\[
I_O = -\alpha I_{in} + \varepsilon,
\]  

(4)

where \( \alpha \) and \( \varepsilon \) are current gain and error term, respectively. By straightforward analysis of circuit in Fig. 3, we will obtain the \( \alpha \) and \( \varepsilon \) as

\[
\alpha = \frac{g_{m5}g_{m17}}{g_{m16}(g_{m2} + g_{m5})} + \frac{g_{m2}g_{m11}}{g_{m10}(g_{m2} + g_{m5})}
\]  

(5)

and

\[
\varepsilon = \left\{ \frac{I_{B1}g_{m5}g_{m17}}{g_{m4}g_{m16}I_{B1}} - \frac{I_{B1}g_{m2}g_{m11}}{g_{m10}I_{B1}} \right\} + \left\{ \frac{g_{m2}}{g_{m1}} - \frac{g_{m5}}{g_m} \right\} \frac{g_{m5}g_{m17}}{g_{m16}} \frac{g_{m2}}{g_{m4}} + \left\{ \frac{g_{m2}g_{m11}}{g_{m10}} \right\} \times \left\{ \frac{g_{m5}g_{m17}}{g_{m16}} + \frac{g_{m2}g_{m11}}{g_{m10}} \right\} \right\}.
\]  

(6)

If \( g_{m1} = g_{m4} \), \( g_{m2} = g_{m5} \), \( g_{m10} = g_{m11} \) and \( g_{m16} = g_{m17} \), then the output current can be shown as

\[
I_O = -I_{in}.
\]  

(7)
terminals and error term, respectively. The output resistance looking into the z terminal (r_z) can be, respectively, expressed as

$$r_z \approx \frac{r_{o13}r_{o19}}{r_{o13} + r_{o19}}.$$  

2.3. Transconductance amplifier

In this section, a simple differential pair amplifier [7] is employed to achieve simpler circuit description of the proposed CCCDT A as shown in Fig. 5.

From Fig. 5, transistors M22 and M23 function as a differential amplifier to convert an input voltage to an output current. M24 and M25 work as a simple current mirror when I_{B2} is an input bias current. When V_{in} is applied, this makes I_{D22} and I_{D23} flowing in M22 and M23, respectively. The relationship of I_o and V_{in} of the transconductance amplifier is given by

$$I_o = \beta_1 g_{m22} V_1 - \beta_2 g_{m23} V_2 + \varepsilon,$$  

where \(\beta_1\) and \(\beta_2\) are transconductance deviations. By straightforward analysis of circuit in Fig. 5, we will obtain the \(\beta_1\), \(\beta_2\) and \(\varepsilon\) as

$$\beta_1 = \frac{g_{m25}}{g_{m24}} + \frac{(g_{m23} g_{m24} - g_{m22} g_{m25})}{g_{m24}(g_{m22} + g_{m23})},$$  

and

$$\beta_2 = 1 - \frac{(g_{m23} g_{m24} - g_{m22} g_{m25})}{g_{m24}(g_{m22} + g_{m23})},$$  

and

$$\varepsilon = - \frac{I_B (g_{m23} g_{m24} - g_{m22} g_{m25})}{g_{m24}(g_{m22} + g_{m23})}.$$  

If \(g_{m22} = g_{m23} = g_m\) and \(g_{m24} = g_{m25}\), Eq. (18) can be reexpressed as

$$I_o = g_m (V_1 - V_2).$$  

In practice implementation, the V_{2} node is grounded and V_{1} is connected to the z terminal. Thus, the output current is
modified to
\[ I_0 = g_m V_z, \quad (23) \]
where
\[ g_m = \sqrt{\beta A I_{B2}}. \quad (24) \]

The output resistance looking into the x terminal \( r_x \) can be, respectively, expressed as
\[ r_x \approx \frac{r_{o23} r_{o25}}{r_{o23} + r_{o25}}, \quad (25) \]
where \( r_o \) is the drain-source resistance seen at the mentioned output terminal.

3. Simulation results

To prove the performances of the completely proposed CCCDTA as shown in Fig. 6, the PSPICE simulation program was used for the examinations. The PMOS and NMOS transistors employed in the proposed circuit were simulated by using the parameters of a 0.35 \( \mu \)m TSMC CMOS technology [8] with \( \pm 1.5 \) V supply voltages. The aspect transistor ratios of PMOS and NMOS are listed in Table 1. Fig. 7 depicts the parasitic resistances at p and n input terminals when \( I_{B1} \) is varied. Fig. 7(a) and (b) were applied by \(+100 \) mV, \(-100 \) mV, respectively. It is seen that the adjustable \( I_{B1} \) current for controllable parasitic resistances is about 10 nA–180 \( \mu \)A range and the resistances due to positive and negative input voltages are slightly different. The bias current more than 180 \( \mu \)A affects MOS transistors operation to saturate and then the CCCDTA cannot be controlled by the input parasitic resistances. Fig. 8 displays DC transfer characteristics of the proposed CCCDTA, when \( I_{B1} = 100 \) \( \mu \)A. So it is clearly seen that it is linear in \(-100 \) \( \mu \)A < \( I_d(I_p) < 100 \) \( \mu \)A and can be adjusted. The offset currents are shown in Fig. 9, when \( I_{B1} \) is varied from 0 to 100 \( \mu \)A. It can be found that the maximum offset current is less than 80 nA. Fig. 10 shows the transconductance value when \( I_{B2} \) is varied from 0 to 200 \( \mu \)A. The obtained
maximum transconductance is about 1 mS. Fig. 11 shows the transient responses of the CCCDTA, it is seen that the switching time delay is about 2 ns. Moreover, the bandwidths of output terminals are shown in Fig. 12. The $-3 \text{ dB}$ cutoff frequencies of the current gains $I_2/I_n$, $I_2/I_p$, $I_x/I_n$ and $I_x/I_p$ are, respectively, located at 282, 311, 50 and 142 MHz, when $I_{B1} = I_{B2} = 100 \mu A$. The proposed CCCDTA properties are concluded in Table 2.

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**Fig. 9.** Offset currents relative to $I_{B1}$.

**Fig. 10.** Transconductance value relative to $I_{B2}$.

**Fig. 11.** Transient responses of the CCCDTA.

**Fig. 12.** Frequency responses at output terminals: (a) $z$ terminal and (b) $x$ terminal.
Table 2. Conclusions of CCCDTA parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption</td>
<td>1.48 mW</td>
</tr>
<tr>
<td>−3 dB Bandwidth</td>
<td>282 MHz (Iz/Iin),</td>
</tr>
<tr>
<td></td>
<td>311 MHz (Iz/Ip),</td>
</tr>
<tr>
<td></td>
<td>50 MHz (Iz/Ih),</td>
</tr>
<tr>
<td></td>
<td>142 MHz (Iz/Ip)</td>
</tr>
<tr>
<td>Input current linear range</td>
<td>−100 µA to 100 µA</td>
</tr>
<tr>
<td>Rn and Rp ranges</td>
<td>821 Ω−25.1 kΩ</td>
</tr>
<tr>
<td>Input bias current range for controlling Rn and Rp</td>
<td>10 nA to 180 µA</td>
</tr>
<tr>
<td>Transconductance</td>
<td>0.25–1 mS</td>
</tr>
<tr>
<td>Switching delay</td>
<td>2 ns</td>
</tr>
<tr>
<td>Input bias range for controlling transconductance amplifier</td>
<td>1 nA to 100 µA</td>
</tr>
<tr>
<td>Rz</td>
<td>1.03 MΩ</td>
</tr>
<tr>
<td>Rx</td>
<td>999.01 kΩ</td>
</tr>
</tbody>
</table>

4. Application examples

4.1. Current-mode biquad filter

The first application of the proposed CCCDTA is a current-mode biquad filter shown in Fig. 13. It employs only one active element and 2 grounded capacitors, which is easy to fabricate, differing from previous circuits [9,10]. The modified version of the CCCDTA to the multiple output is used, the internal realization is shown in Fig. 14, where currents Iz2 and Iz3 are the opposite direction from Iz1. Considering at node 1, it yields

\[ I_{in} = I_{HP} + i_n + I_{LP}, \]  

where \( V_{C1} = I_{HP}/sC_1 \). The current at z1 terminal can be expressed as

\[ I_{z1} = I_{BP} = -I_{z2} = -I_{z3} = i_n = \frac{V_{C1}}{R_n} = \frac{I_{HP}}{sC_1R_n}. \]  

The voltage at z terminal can be shown as

\[ V_{z1} = \frac{I_{z1}}{sC_2} = \frac{I_{HP}}{s^2C_1C_2R_n}. \]  

The \( I_{LP} \) can be found as

\[ I_{LP} = g_m V_z = \frac{I_{HP}g_m}{s^2C_1C_2R_n}. \]  

Substituting Eqs. (27) and (29) into (26), it yields

\[ I_{in} = I_{HP} \left( 1 + \frac{1}{sC_1R_n} + \frac{g_m}{s^2C_1C_2R_n} \right). \]  

So, the high-pass, low-pass and band-pass functions can be respectively expressed as

\[ \frac{I_{HP}}{I_{in}} = \frac{s^2}{s^2 + \frac{1}{C_1R_n} + \frac{g_m}{C_1C_2R_n}}, \]  

\[ \frac{I_{LP}}{I_{in}} = \frac{g_m/C_1C_2R_n}{s^2 + \frac{1}{C_1R_n} + \frac{g_m}{C_1C_2R_n}}, \]  

and

\[ \frac{I_{BP}}{I_{in}} = \frac{s}{C_1R_n}. \]  

Moreover, the band-stop and the all-pass functions can be obtained from the currents \( I_{BS} = I_{in} - I_{BP}, I_{AP} = I_{BS} - I_{BP} \), respectively, as following equations:

\[ \frac{I_{BS}}{I_{in}} = \frac{s^2 + g_m/C_1C_2R_n}{s^2 + \frac{1}{C_1R_n} + \frac{g_m}{C_1C_2R_n}}, \]  

and

\[ \frac{I_{AP}}{I_{in}} = \frac{s^2 - s/C_1R_n + g_m/C_1C_2R_n}{s^2 + \frac{1}{C_1R_n} + \frac{g_m}{C_1C_2R_n}}. \]  

The pole frequency \( \omega_0 \) and the quality factor \( Q_0 \) are

\[ \omega_0 = \sqrt{\frac{g_m}{C_1C_2R_n}}, \quad Q_0 = \sqrt{\frac{C_1g_mR_n}{C_2}}. \]  

Substituting the intrinsic resistance and transconductance as depicted in Eqs. (3) and (24), it yields

\[ \omega_0 = \left( \frac{\beta n \sqrt{8I_{B1}I_{B2}}}{C_1C_2} \right)^{1/2}, \quad Q_0 = \left( \frac{C_1 \sqrt{I_{B2}}}{C_2 \sqrt{8I_{B1}}} \right)^{1/2}. \]  

From Eq. (37), it can be remarked that the pole frequency can be adjusted by \( I_{B1} \) and \( I_{B2} \) without affecting the quality factor by keeping the ratio \( I_{B1} \) and \( I_{B2} \) to be constant.
The confirmed results of several obtained functions can be seen in Fig. 15, by setting $C_1 = C_2 = 1 \text{nF}$ and $I_{B1} = I_{B2} = 50 \mu\text{A}$. Fig. 16 shows phase and magnitude responses for all-pass function. The results in Fig. 17 show that the pole frequency and the quality factor can be electronically adjusted as depicted in Eq. (37). Fig. 18 shows magnitude responses of band-pass function where $I_{B1}$ and $I_{B2}$ are equally set and changed for several values, by keeping its ratio to be constant. It is found that pole frequency can be adjusted without affecting the quality factor.

4.2. Floating inductance simulator

Fig. 19 depicts the proposed floating inductance simulator, where $I_{B1}$ and $I_{B2}$ are input bias currents of CCCDTA. Considering the circuit in Fig. 19 and using CCCDTA properties in Section 2, we will receive

$$I_z = \frac{V_1 - V_2}{R},$$  
$$V_z = \frac{I_z}{sC} = \frac{V_1 - V_2}{sCR}.$$  
$$I_x = I_L = \frac{g_m(V_1 - V_2)}{sCR}.$$  

From Eq. (40), an input impedance of the circuit can be written as

$$Z_{in} = \frac{V_1 - V_2}{I_L} = \frac{sCR}{g_m}. \quad (41)$$

It is obvious that, from Eq. (41), the circuit shown in Fig. 19 simulates a floating inductance with a value

$$L_{eq} = \frac{CR}{g_m} = \frac{1}{\beta_n \sqrt{8I_{B1}I_{B2}}}. \quad (42)$$

It is clearly seen that, from Eq. (42), the inductance value $L_{eq}$ can be electronically adjusted by either $I_{B1}$ or $I_{B2}$. For non-ideal case, assuming that no error term occurs in the CCCDTA, the $I_z$ and $I_x$ of CCCDTA can be, respectively, characterized by

$$I_z = x_p I_p - x_n I_n \quad (43)$$
and
$$I_x = \beta_z g_m V_z. \quad (44)$$

While the output voltage of voltage buffer can be characterized by

$$V_o = \beta_b V_{in}, \quad (45)$$
where $x_i$ and $\beta_i$ are current gain and voltage gain errors of CCCDTA and voltage buffer, respectively. Taking into account, $x_i$ and $\beta_i$ effect on the circuit in Fig. 19, it can be found that

$$I_L = \frac{g_m \beta_z}{sCR} (x_n \beta_{b1} V_1 - x_p \beta_{b2} V_2), \quad (46)$$
where $x_n \beta_{b1} = x_p \beta_{b2} = \kappa$, the input impedance can be rewritten as

$$Z_{in} = \frac{V_1 - V_2}{I_L} = \frac{sCR}{\kappa g_m \beta_z}. \quad (47)$$

From Eq. (47), for non-ideal consideration, the circuit in Fig. 19 simulates a floating inductance with a value

$$L_{eq} = \frac{CR}{\kappa g_m \beta_z}. \quad (48)$$
If these error factors are close to unity, the deviations of the inductance value in Eq. (48) can be neglected. Fig. 20 shows the circuit description of voltage buffer used for the simulation. Fig. 21 shows the typical waveforms of the voltage and current through the proposed floating inductor in Fig. 19, when $I_{B1} = I_{B2} = 100 \mu A$. The impedance of the simulator relative to frequency, compared to ideal inductor, is also shown in Fig. 22. Fig. 23 shows impedance values relative to frequency of the simulator with different $I_{B2}$. To illustrate an application of the floating inductance simulator, it is employed in an RLC series-resonant circuit shown in Fig. 24, where $V_{in} = 10 \text{ mV}$. The frequency responses of output current $I_o$ for different $I_{B2}$ are shown in Fig. 25.

4.3. Quadrature oscillator

The last application of proposed CCCDTA is a quadrature oscillator shown in Fig. 26. It consists of one multiple output CCCDTA (MO-CCCDTA) and 2 grounded capacitors. The MO-CCCDTA properties are similar to CCCDTA, except that

$$I_{z1} = I_{z2} = I_p - I_n, \quad (49)$$

$$I_{x1} = g_m^1 V_{z1}, \quad (50)$$

and

$$I_{x2} = g_m^2 V_{z2}, \quad (51)$$

where $g_m^1 = \sqrt{\beta_n I_{B2}}$ and $g_m^2 = \sqrt{\beta_n I_{B3}}$. Considering the circuit in Fig. 26 and using the MO-CCCDTA properties, it yields characteristic equation of this circuit as

$$s^2 + s \frac{1}{C_1} \left( \frac{2}{R_p} - g_m^2 \right) + \frac{g_m^1}{C_1 C_2 R_p} = 0. \quad (52)$$

From Eq. (52), it is obviously seen that the proposed circuit can be set to be an oscillator if

$$\frac{2}{R_p} = g_m^2. \quad (53)$$
Fig. 21. Typical waveforms of voltage and current of the proposed inductor simulator.

Fig. 22. The impedance values relative to frequency of the simulator.

Fig. 23. The impedance values relative to frequency of the simulators with different $I_{B2}$.

Fig. 24. Series RLC resonant circuit.

Eq. (53) is called as condition of oscillation, this is achieved by setting $I_{B1} = 0.25 I_{B3}$, then the characteristic equation of the system becomes

$$\lambda^2 + \frac{g_{m1}}{C_1 C_2 R_p} = 0.$$  \hspace{1cm} (54)

From Eq. (54), the oscillation frequency of this system can be obtained as

$$\omega_0 = \sqrt{\frac{g_{m1}}{C_1 C_2 R_p}} = \left( \frac{\beta_n \sqrt{8 I_{B1} I_{B2}}}{C_1 C_2} \right)^{1/2}.$$  \hspace{1cm} (55)
It can be seen that, from Eq. (55), the oscillation frequency \((\omega_0)\) can be controlled by bias current. From Eqs. (53) and (55), it should be remarked that the condition of oscillation can be tuned by \(I_{B3}\) without affecting the oscillation frequency which can be adjusted by \(I_{B1}\) and \(I_{B2}\). Furthermore, the quadrature sinusoidal signals can be obtained at \(I_{O1}\) and \(I_{O2}\) or \(V_{O1}\) and \(V_{O2}\) of Fig. 26, in current-mode and voltage-mode, respectively, with the same time. For non-ideal case, the \(I_x\) and \(I_z\) of MO-CCCDTA can be, respectively, characterized by

\[
I_{x1} = z_{p1} I_p - z_{n1} I_n, \quad (56)
\]

\[
I_{x2} = z_{p2} I_p - z_{n2} I_n, \quad (57)
\]

\[
I_{x1} = \beta_1 V_{z1} \quad (58)
\]

and

\[
I_{x2} = \beta_2 V_{z2}, \quad (59)
\]

where \(z_p, z_n\) and \(\beta\) are transferred error values deviated from one. In the case of non-ideal and brief consideration, the \(\omega_0\) is changed to

\[
\omega_0 = \sqrt{\frac{z_{p1} z_{n1}}{C_1 C_2 R_P}} \quad (60)
\]

The confirmed results of quadrature oscillator can be seen in Figs. 27–29. They show the responses of quadrature oscillator with bias currents: \(I_{B1}\), \(I_{B2}\) and \(I_{B3}\) are respectively, set to 20, 100 and 81 µA, where the total harmonic distortion (THD) is about 0.892%.

5. Conclusions

The new building block, called as CCCDTA, has been introduced in this paper. The usabilities have been proven by the simulations and application examples. They consume few numbers of components while electronic controllability is still available, which superior to the recently proposed circuits. This novel element is very appropriate to realize in a commercially-purposed integrated circuit. Our future work is to find more applications of the CCCDTA, emphasizing on current-mode signal processing circuits.

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References

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