A Synthesis of Temperature Insensitive/Electronically Controllable Floating Simulators Based on DV-CCTAs

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Abstract - A circuit topology for synthesis of floating inductance, floating capacitance multiplier and floating frequency dependent negative resistance (FDNR) conversion depending on the external passive component selection is proposed in this paper. The proposed simulator employs 2 differential voltage current conveyor transconductance amplifiers (DV-CCTAs) and only 3 grounded passive elements without component matching requirements. The simulated component values can be adjusted electronically by input bias currents of the DV-CCTAs and are temperature-insensitive. The application example as a bandpass filter is included. The simulation results using PSPICE are given for the introduced floating simulator to verify the theory and to exhibit the performances of the circuit.

I. INTRODUCTION

Recently, a simulated immittance has become a standard research topic since it can be applied in areas like oscillator design, active filters and cancellation of parasitic elements [1-2]. The advent of integrated circuits has encouraged the design of synthetic inductances, which can be used instead of the bulky inductors in passive filters. Although, it is difficult to implement inductors and floating capacitors in the integrated circuits, several published circuits employing different high-performance active building blocks.

The literature surveys show that a large number of circuit realizations for floating simulators have been reported [2-15]. Unfortunately, these reported circuits suffer from one or more of following weakness
- Need for matching passive elements [7-8, 12].
- Lack of electronic adjustability [3, 5-6, 8, 10-13].
- Use of floating capacitors, which is not convenient to further fabricate in IC [3-6, 10-13].
- The obtained impedance values are temperature sensitive [2-15].
- Require changing circuit topologies to achieve several functions [2].

As a solution, the circuit topology for simulation of a floating inductance, capacitance and FDNR depending on the external passive element choice is presented. The proposed circuit consists of DV-CCTAs as active components, which is slightly modified from the recently proposed CCTA [16]. The DV-CCTA is an interesting active building block, because it can be employed to synthesize and design the modern electronic circuits and systems employing only a few numbers of elements. In this paper, the proposed topology employs 2 DV-CCTAs cooperating with three grounded as external passive components. The circuit can synthesize a lossless floating inductance, capacitance and FDNR without changing the original topology. Practically, in this design, all of synthesized immittance values can be electronically adjusted by input bias currents of the DV-CCTAs and are temperature-insensitive. Furthermore, the effects of non-ideal gains of the proposed simulator are considered. The PSPICE simulation results are also shown, they are in correspondence with the theoretical analysis.

II. PRINCIPLE AND OPERATION

A. The Differential Voltage Current Conveyor Transconductance amplifiers (DV-CCTA)

The DV-CCTA whose electrical symbol and equivalent circuit are shown in Fig. 1, is a five-terminals network. Each terminal has ideal characteristics described by following equation

\[
\begin{bmatrix}
I_{t1} \\
I_{t2} \\
V_x \\
I_s \\
I_o
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 & I_x \\
0 & 0 & 0 & 0 & V_{t1} \\
0 & 1 & -1 & 0 & V_{t2} \\
1 & 0 & 0 & 0 & V_s \\
0 & 0 & \pm g_m & 0 & V_o
\end{bmatrix}
\begin{bmatrix}
0 \\
0 \\
1 \\
0 \\
0
\end{bmatrix}.
\]

\(g_m\) is the transconductance gain of DV-CCTA. For a bipolar DV-CCTA, the transconductance gain can be expressed by

\[g_m = \frac{I_o}{2V_t},\]

where \(I_o\) and \(V_t\) are bias current and thermal voltage, respectively.
Proposed floating simulator

The proposed floating simulator is shown in Fig. 2, where $I_{B1}$ and $I_{B2}$ are input bias currents of DV-CCTA1 and DV-CCTA2, respectively. Straightforwardly analyzing circuit in Fig. 3, an input impedance of the proposed circuit can be written as

$$Z_m = V_1 - V_2 = \frac{g_mZ_1Z_2}{g_mZ_2}. \tag{3}$$

Substituting the transconductance gain as shown in Eq. (2) into Eq. (3) the input impedance is subsequently shown as

$$Z_m = \frac{I_{B2}Z_1Z_2}{I_{B1}Z_2}. \tag{4}$$

We can found that, if the connected component is free from temperature, the obtained component value is temperature-insensitive and can be adjusted by any input bias currents.

Considering Eq. (4), the following passive elements are chosen to achieve floating inductance, floating capacitance and floating frequency dependent negative resistance (FDNR).

In addition, they can be adjusted electronically by input bias currents of the DV-CCTAs and are temperature-insensitive, as following explained.

(a) If $Z_1 = 1/sC_1$, $Z_2 = R_2$ and $Z_3 = R_3$ are taken for the circuit in Fig. 3 the input impedance of floating capacitance multiplier is found to be

$$Z_m = \frac{I_{B2}R_2}{sC_1I_{B1}R_2} = \frac{1}{sC_{eq}}. \tag{5}$$

Hence, $C_{eq} = C_1I_{B1}R_2/I_{B1}R_1$.

(b) If $Z_1 = R_1$, $Z_2 = R_2$ and $Z_3 = 1/sC_1$ are taken for the input impedance of floating capacitance multiplier is found to be

$$Z_m = \frac{I_{B2}R_2}{sC_1I_{B1}R_2} = \frac{1}{sC_{eq}}. \tag{6}$$

Hence, $C_{eq} = C_1I_{B1}R_2/I_{B1}R_1$.

c) If $Z_1 = R_1$, $Z_2 = 1/sC_2$, $Z_3 = R_3$ are taken for the input impedance of floating inductance simulator is found to be

$$Z_m = \frac{sC_2I_{B2}R_3}{I_{B1}} = sL_{eq}. \tag{7}$$

Hence, $L_{eq} = C_2I_{B2}R_3/I_{B1}$.

d) If $Z_1 = 1/sC_1$, $Z_2 = R_2$, $Z_3 = 1/sC_3$ are taken for the input impedance of floating FDNR simulator is found to be

$$Z_m = \frac{I_{B2}}{s^2C_1C_2I_{B1}R_2} = \frac{1}{s^2D_d}. \tag{8}$$

Consequently, $D_d = I_{B2}/C_1C_2I_{B1}R_2$ is obtained. As frequency increase, the absolute value of negative resistance decrease.

C. Analysis of non-ideal case

For non-ideal case, the DV-CCTA can be respectively characteristic with the following equation

$$
\begin{bmatrix}
I_{y1} \\
I_{y2} \\
V_x \\
I_z \\
I_o
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
\gamma & 0 & -\gamma & 0 \\
\alpha & 0 & 0 & 0 \\
0 & 0 & \pm\beta g_m & 0
\end{bmatrix}
\begin{bmatrix}
I_x \\
V_{y1} \\
V_{y2} \\
V_x \\
V_o
\end{bmatrix}.
$$
\tag{9}

561
\[ \alpha, \beta \text{ and } \gamma \text{ are the frequency dependent voltage gains, these gains are ideally equal to unity.} \]

In the case of non-idea, the input impedance in Eq. (4) is converted to

\[
Z_m = \frac{V_i - V_o}{I_{in}} = \frac{\alpha_1 g_{m1} Z_1 + \beta_1 g_{m2} Z_2}{\alpha_1 g_{m1} + \beta_1 g_{m2}}.
\] (10)

Practically, the \( \alpha_1, \beta_1 \) and \( \gamma \) originate from the intrinsic resistances and stray capacitances in transistors used in the considering DV-CCTA. These errors affect the sensitivity to temperature, especially at high frequency range and the high frequency response of the proposed circuit, then the DV-CCTA should be carefully designed in transistor-level to minimize these errors. Consequently, these deviations are very small and can be ignored in theory.

III. SIMULATION RESULTS

To prove the performance of the proposed simulator, the PSPICE simulation program was used for the examination. The PNP and NPN transistors employed in the proposed topology were simulated by respectively using the parameters of the PR200N and NR200N bipolar transistors of ALA400 transistor array from AT&T [17]. The DV-CCTA employed in the proposed simulator topology were simulated with \( \pm 2.5V \) supply voltages, where input bias currents; \( I_{B1} = 100\mu A \), \( I_{B2} = 100\mu A \), and \( I_{B2} = 200\mu A \). Fig. 3 depicts schematic description of the DV-CCTA used in the simulations.

Figure 3. Internal construction of DV-CCTA.

Phase and magnitude responses for the impedances of the proposed topology in Fig. 2 are given in Fig. 4, where the second port of the floating simulator is grounded. It is seen that, in case of (a), (b) and (c) the useful frequency ranges are about 3kHz to 3MHz and approximately 10kHz to 2MHz for the case (d). Additionally, the claimed temperature-insensitivities of the proposed circuit are confirmed by the results of Fig. 5, depicting simulated inductance response.

Figure 4. Phase and impedances of the proposed circuit when the second port is grounded.

Figure 5. Simulated characteristics of inductance simulator for different temperatures.
An application of the floating inductance simulator obtained from the proposed topology to a bandpass filter is also shown to verify the performances, as shown in Fig. 6. From the results in Fig. 7, in addition, we found that the center frequencies can be adjusted by varying the input bias current of the DV-CCTAs. Furthermore, the claimed temperature-insensitivities of the proposed topology in the bandpass filter are confirmed by the result in Fig. 8.

\[ I_{BI_1} \]  
\[ C = 4nF \]  
\[ V_o \]  
\[ V_i \]  
\[ R = 100\Omega \]  

Figure 6. A bandpass filter example.

\[ \text{Magnitude(V)} \]  
\[ \text{Frequency(Hz)} \]  
\[ I_{BI_1} = 100\mu A \]  
\[ I_{BI_1} = 200\mu A \]  
\[ I_{BI_1} = 300\mu A \]  

Figure 7. Simulated characteristics of bandpass response for different \( I_{BI_1} \).

\[ \text{Magnitude(V)} \]  
\[ \text{Frequency(Hz)} \]  
\[ 25^\circ C \]  
\[ 75^\circ C \]  
\[ 100^\circ C \]  

Figure 8. Simulated characteristics of bandpass response for different temperatures.

IV. CONCLUSIONS

The circuit topology for synthesis of floating inductance, floating capacitance multiplier and floating frequency dependent negative resistance (FDNR), depending on the passive component selection has been proposed in this paper. The proposed simulator employs 2 DVCCCTAs and only 3 grounded passive elements without component matching requirements. The simulated component values can be adjusted electronically by input bias currents of the DV-CCTAs and are temperature-insensitive, which have been confirmed through PSPICE. The application example of the inductance simulator obtained from the proposed topology as a bandpass filter is included. It can well verify the performances of the proposed topology.

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