TWO LOW-VOLTAGE HIGH-SPEED CMOS FREQUENCY-INSENSITIVE PWM SIGNAL GENERATORS BASED ON RELAXATION OSCILLATOR

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ABSTRACT

In this paper, two new simple PWM (Pulse Width Modulation) signal generators based on modified CMOS relaxation oscillator are introduced. Translinear current dividers are proposed to improve the circuit performance such that it is frequency insensitive to the magnitude of an input signal. In addition, the precise PWM signal can be easily achieved under low voltage consumption and the output frequency can be ranged up to several megahertz. Furthermore, both voltage and current modulating signal can be applied. Based on the features and the simplicity of the circuits, it is very suitable for developing into Integrated Circuits (ICs) form in communication applications. The simulation results through PSPICE show a good agreement with theoretical anticipation.

1. INTRODUCTION

A PWM signal is widely utilized in the areas of power electronics, instrumentation and communication systems, especially in optical communication. By the reason, the PWM signal generator has been realized in Integrated Circuits (ICs) form that makes it conveniently implemented. However, the circuit configuration is typically composed of current sources, flip-flop, comparators and analog switches as well [1]. It causes inevitably comprising of a bulk of transistors. Although, the recent literatures have proposed the simple PWM signal generators [2-3], the schemes have limitations in such maximum frequency of PWM output signal due to a slow rate of an active element and high supply voltage of operation. In addition, the duty cycle of PWM output signal does not linearly vary with modulating signal. They have subsequently some distortion after demodulation. Alternatively, a low-voltage high-speed PWM signal generations based on BJT relaxation oscillator has been introduced [4]. However, its PWM output frequency is dependent on squaring of an input signal frequency, causing a distortion in demodulation process.

The purpose of this article is to present 2 new low-voltage PWM signal generators modified from the CMOS relaxation oscillator. The benefit of the proposed circuits is that they can yield the precise PWM output signal whose duty cycle is linearly dependent on a magnitude of the modulating (information) signal over a high-speed and low-voltage. In addition, by using CMOS translinear current divider, the PWM output frequency is insensitive to magnitude of an input signal and adjustable based on a bias current in the current divider section. In accordant of mathematical derivation, the circuit performances are also proved here through PSPICE simulations.

2. PRINCIPLE

2.1 The conventional CMOS relaxation oscillator

The relaxation oscillators using source-coupled connection of CMOS are widely utilized in many areas, especially in communications [5] due to their abilities in high frequency performance. This causes them to be suitably developed into Voltage Controlled Oscillators (VCOs) and Current Controlled Oscillators (CCOs) forms [6-7]. Fig. 1 is a simplified diagram of a CMOS relaxation oscillator circuit demonstrating the presented principle. The circuit is derived from the source-coupled multivibrator configuration and can provide a square-wave output. Its operation can be briefly explained as follows.

![Fig. 1 The classical CMOS relaxation oscillator circuit](image)

$M_1$ and $M_2$ act as a gain stage. At any given time $M_1$ and $M_2$ or $M_3$ and $M_4$ are conducting, such that the capacitor $C$ is alternately charged and discharged by constant current $I$. The output across $M_3$ and $M_4$ corresponds to a symmetrical square wave, with a peak-to-peak amplitude of $2V_{GST}$, where $V_{GST}$ is the MOS transistor threshold voltage. The output $V_{S1}$ is a constant when $M_1$ is on, and becomes a linear ramp with a slope equal to $(-I/C)$ when $M_1$ is off. The output $v_{S2}(t)$ is the same as $v_{S1}(t)$, except for a half-cycle delay. Both of these linear ramp waveforms have peak-to-peak amplitudes of $2V_{GST}$. The frequency of oscillation can be expressed as

$$f_o = \frac{I}{4V_{GST}C} \quad (1)$$

2.2 The proposed principle

The PWM signal output can be obtained by adjusting the charged and discharged constant current values to make them...
linearly dependent on a modulating signal. It can be achieved by adding 2 translinear current controlled current dividers as shown in Fig 2, which have an output current dependent on the modulating (information) signal. From the principle, it found that during positive voltage interval of the PWM signal output, \( M_3 \) is on and \( M_4 \) is off. Fig. 3 shows circuit detail of the current divider using translinear principle [8]. The current charging the capacitor is an \( I_{L2} / [I_{L} + i_{in}(t)] \) where \( i_{in}(t) \) is an instantaneously modulating signal.

\[ D(\%) = \frac{I_S + i_{in}(t)}{2I_S} \times 100\% \quad (7) \]

It means that, from equation (7), the duty cycle of the PWM output signal would be a 50% if \( i_{in}(t) = 0 \), which agrees with the mostly typical applications. It is also discernibly shown that, besides, the duty cycle is linearly dependent on the modulating signal.

2.3 The first proposed circuit

Fig. 4 shows the first proposed circuit generated from the PWM signal generation in Fig. 2. One conventional current mirror (CM) is used to copy the information signal; \( I_{in}(t) \) to the current divider as a current source. Another CM is used as a current sink of \( I_{in}(t) \). In this circuit, it should be noted that the modulating signal must be more than zero for maintaining current mirrors to work continuously.

2.4 The second proposed circuit

With the first circuit, however, the modulating signal is limited as a positive current and the only more than 50% duty cycle can be received at the PWM output terminal. The modulating signal in voltage form can be applied to the PWM signal generator using the second circuit shown in Fig. 5. A CMOS multiple output second generation current conveyor \((CCII \pm)\) is utilized to function as a voltage to current converter. The modulating signal can be positive or negative range if the proposed circuit is biased with dual supply voltages. Thereby, the variable duty cycle of 0-100% can be achieved.
3. PERFORMANCE ANALYSIS

In section 2, the proposed circuits function in ideal circuit operation. Practically, however, the principal error of the proposed circuit stems from several practical characteristics of the current mirror [9] as shown in Fig. 6 employing in the CCI and sub-circuits. These characteristics affect deviations of the frequency of the PWM output signal.

![Fig. 6 Current mirror employing in proposed circuits](image)

### 3.1 Input and output resistance

An ideal current mirror has zero input resistance and infinite output resistance. Consequently, the input voltage does not vary with the input current and the output current is independent of the output voltage. However, actual current mirror have non-zero input resistance and non-infinite output resistance which cause an error in the output current as

\[ I_{OUT} \approx I_{IN} \frac{1 + \frac{R_{DS}}{R_{out}}} {1 + \frac{R_{DS}}{R_{out}}} \approx I_{IN} \left(1 - \varepsilon\right) \]  

(8)

Where \( \varepsilon \) is the systematic gain error,

\[ \varepsilon = \frac{R_{DS}}{R_{out}} \]  

(9)

The error in the output current may be expressed as:

\[ \Delta I = I_{IN} - I_{OUT} \approx I_{IN} \left(\frac{1}{I_{OUT}} - \frac{1}{1 - \varepsilon}\right) \]  

(10)

Therefore, the error current can be reduced by minimizing the ratio of the output resistance to the output resistance.

### 3.2 Input linear range

For the accurate reproduction of the signal current at the current mirror output, the input current must be in the range where both devices operate in saturation at all times. A peak current that is 50% of the bias current level generally provides a reasonable compromise between power dissipation and dynamic range.

### 3.3 DC-balance

The drain-source voltages of the mirror transistors also affect the accuracy of the output current. If the devices are biased in saturation and by assuming that all the process-dependent parameters are identical, the ratio of the currents is

\[ \frac{I_{OUT}}{I_{IN}} = 1 + \frac{\lambda V_{DS}}{1 + \lambda V_{DS}} \]  

(11)

Thus for \( \lambda V_{DS} \ll 1 \), \( \lambda \) is a channel-length modulation effect, the error in the output current due to \( V_{DS} \) mismatch is

\[ I_{error} = \lambda (V_{DS2} - V_{DS1}) \]  

(12)

Clearly, if the drain-source voltages of \( M_1 \) and \( M_2 \) are unequal, there will be an offset in the output current.

In summary, the error of PWM output frequency can be expressed as

\[ f = \frac{I_{I_{OUT}}}{4I_{IN}V_{DS}^{2}(1 - \varepsilon)} \]  

(13)

Where the duty cycle of PWM output signal is independent of this error.

4. SIMULATION RESULTS

To prove the performances of the proposed circuits, PSPICE simulation program has been used, the CMOS transistors were simulated using a standard BSIM3V3.1 CMOS model [10]. The aspect ratios \( W/L \) of the all of transistor are 50\( \mu m / 0.5 \mu m \). The power supply voltage was 2V applied to the first circuit. The passive elements are 10pF capacitor and 10\( k\) resistors. For, the first result of the first circuit, the duty cycle and frequency of PWM output signal versus DC modulating current variations is shown in Fig. 6. It should be noted that the duty cycle of the PWM output signal is linearly dependent on the magnitude of modulating signal followed by eqn. (7) whereas its frequency deviation is maintained to less than 5%.

![Fig. 6 Static characteristics of first proposed PWM signal generator](image)

![Fig. 7 The simulated results of the sinusoidal modulating input of the first circuit relative to the PWM output signal](image)
PWM Frequency Deviation (%)
4.8mW, respectively, while the highest PWM output frequency is approximately 700MHz.

5. CONCLUSIONS

Two CMOS PWM signal generators based on modified relaxation oscillator scheme have been introduced. The proposed circuits gain the precision of PWM signal output whose duty cycle linearly depends on the magnitude of a modulating signal with a high-speed and low-voltage power supply. The modulating (information) signal in current form can be applied to the first circuit while the modulating signal in voltage form can be fed to the second circuit. In addition, the modulating current signal is available in the second circuit by feeding current signal to the X terminal whereas the Y terminal is connected to ground. Due to the simplicity of the circuit details, they are very suitable to fabricate into an integrated circuit form through CMOS technology. The main applications of these circuits are in the high-speed optical transmission systems [12] or digital to analog conversion [13].

6. REFERENCES