Chapter 19

TRADE-OFFS IN OSCILLATOR PHASE NOISE

Ali Hajimiri
California Institute of Technology

19.1. Motivation
The frequency spectrum is a valuable commodity as the ever increasing number of wireless users demand more efficient usage of the already scarce frequency resources. Communication transceivers rely heavily on frequency conversion using local oscillators (LOs) and, therefore, the spectral purity of the oscillators in both the receiver and the transmitter is one of the factors limiting the maximum number of available channels and users. For that reason, a deeper understanding of the fundamental issues limiting the performance of oscillators, and development of design guidelines to improve them, are necessary [1–48].

In digital applications, the timing accuracy of the clock signal determines the maximum clock rate and hence the maximum number of operations per unit time. In microprocessors and other synchronous very large-scale digital circuits, the clock signal is generated by on-chip oscillators locked to an external oscillator. Ring oscillators are commonly used for on-chip clock generation due to their large tuning range and ease of integration. In the IC environment, there are additional sources affecting the frequency stability of the oscillators, namely, substrate and supply noise arising from switching in the digital circuitry and output drivers. This new environment and the delay-based nature of ring oscillators demand new approaches to the modeling and analysis of the frequency stability of the oscillators.

We will start this chapter with an introduction to the definitions, describing some of the different methods for quantifying frequency instability in an oscillator. Next, we will introduce a time-variant model for phase noise, using impulse sensitivity functions (ISFs), from which the phase response of an oscillator to an arbitrary noise source is determined. Next, we will talk about phase noise trade-offs and design implications in LC and ring oscillators.

19.2. Measures of Frequency Instability
Any practical oscillator has fluctuations in its amplitude and frequency. Short-term frequency instabilities of an electrical oscillator are mainly due to inherent device noise (such as thermal and flicker noise) as well as interference sources (such as supply and substrate noise sources). These sources result in
frequency instabilities. In this section, we give an introduction to frequency instabilities, their destructive effects on the performance of analog and digital systems, and the definitions of jitter and phase noise.

The output of an ideal oscillator may be expressed as $V_{\text{out}}(t) = V_0 \cos(\omega_0 t + \phi_0)$, where the amplitude $V_0$, the frequency $\omega_0$, and phase reference $\phi_0$ are all constants. The one-sided spectrum of an ideal oscillator with no random fluctuations consists of an impulse at $\omega_0$ as shown in Figure 19.1. In a practical oscillator, however, the output is more generally given by

$$V_{\text{out}}(t) = V_0 \cdot [1 + A(t)] \cdot f[\omega_0 t + \phi(t)]$$  \hspace{1cm} (19.1)

where $\phi(t)$ and $A(t)$ are functions of time, $V_0$ is the maximum voltage swing and $f$ is a periodic function which represents the shape of the steady-state output waveform of the oscillator. The output spectrum has power around harmonics of $\omega_0$ if the waveform, $f$, is not sinusoidal. More importantly, as a consequence of the fluctuations represented by $\phi(t)$ and $A(t)$, the spectrum of a practical oscillator has sidebands close to the frequency of oscillation, $\omega_0$, and its harmonics, as shown in Figure 19.1. These sidebands are generally referred to as phase noise sidebands.

The destructive effect of phase noise can be best seen in the front-end of a radio receiver. Figure 19.2 shows a typical front-end block diagram, consisting of a low noise amplifier (LNA), a mixer, and an LO. Suppose the receiver tunes to a weak signal in the presence of a strong signal in an adjacent channel. If the LO has large phase noise, as shown in Figure 19.3, some down-conversion of the interfering signal into the same intermediate frequency (IF) as that of the desired signal will occur as shown in Figure 19.3. The resulting interference significantly degrades the dynamic range of the receiver. Therefore, improving

![Figure 19.1. The spectrum of an ideal and a practical oscillator.](image-url)
the phase noise of the oscillator clearly improves the signal-to-noise ratio of the desired signal.

In the time-domain viewpoint, the spacing between transitions is ideally constant. In practice, however, the transition spacings will be variable due to fluctuations in $\phi(t)$. This uncertainty is known as timing jitter and can be seen in Figure 19.4. In a synchronous digital circuit such as a microprocessor, there is a clock signal that controls the operation of different logic blocks. To emphasize the importance of timing jitter, consider the example of a flip-flop. If the clock signal has zero timing jitter as shown with the solid line in Figure 19.4, the data needs to be stable only for $t_{\text{setup}} + t_{\text{hold}}$. However, if the clock line shows a peak-to-peak jitter of $\tau_{\text{max}}$, then the data line needs to be stable for a period of time $2\tau_{\text{max}}$ longer, as shown in Figure 19.4. This decrease in the timing margins will reduce the maximum achievable frequency of operation for the digital circuit.

The harmful effect of clock jitter can also be seen in the sample-and-hold circuit of Figure 19.5, where the accuracy of the sampling process is affected by jitter in the clock. If there is uncertainty in sampling time (i.e. clock jitter), it translates directly to uncertainty in the sampled value (i.e. noise) as shown in Figure 19.5.
19.2.1. Phase Noise

In the frequency-domain viewpoint, an oscillator’s short-term instabilities are usually characterized in terms of the single sideband noise spectral density. Units of decibels below the carrier per Hertz (dBc/Hz) are conventionally used and is defined as:

\[
L_{\text{total}}(\Delta \omega) = 10 \cdot \log \left( \frac{P_{\text{sideband}}(\omega_0 + \Delta \omega, 1 \text{ Hz})}{P_{\text{carrier}}} \right) \tag{19.2}
\]

where \( P_{\text{sideband}}(\omega_0 + \Delta \omega, 1 \text{ Hz}) \) represents the single sideband power at a frequency offset, \( \Delta \omega \) from the carrier in a measurement bandwidth of 1 Hz as shown in Figure 19.6, and \( P_{\text{carrier}} \) is the total power under the power spectrum. Note that the definition of (19.2) includes the effect of both amplitude and phase fluctuations, \( A(t) \) and \( \phi(t) \).

Spectral density is usually specified at one or a few offset frequencies. To be a meaningful parameter, both the noise density and the offset need to be reported, for example, \(-100 \text{ dBc/Hz} \) at 10 kHz offset from the carrier.
The advantage of \( S_{\alpha}(\omega) \) in (19.2) is its ease of measurement. Its disadvantage is that it shows the sum of both amplitude and phase variations; it does not show them separately. It is often important to know the amplitude and phase noise separately because they behave differently in a circuit. For instance, the effect of amplitude noise can be reduced by amplitude limiting, while the phase noise cannot be reduced in an analogous manner. Therefore, in most practical oscillators, \( S_{\alpha}(\omega) \) is dominated by its phase portion, \( S_{\phi}(\omega) \), known as phase noise, which will be simply denoted as \( S_{\phi}(\omega) \) unless specified otherwise.

If one plots \( S_{\phi}(\omega) \) for a free-running oscillator as a function of \( \omega \) on logarithmic scales, regions with different slopes may be observed as shown in Figure 19.7. At large offset frequencies, there is a flat noise floor. At small offsets, one may identify regions with a slope of \( -1/f^2 \) and \( -1/f^3 \), where the corner between the \( -1/f^2 \) and \( -1/f^3 \) regions is \( \omega_0 \). Finally, the spectrum becomes
flat again at very small offset frequencies. The mechanisms responsible for these features will be discussed in great detail in subsequent chapters.

There are different methods of measuring phase noise and, depending on the particular method used to measure it, parts of the spectrum of Figure 19.7 may or may not be observed. For example, if a spectrum analyzer is used to measure the phase noise, \( \omega_{-3\text{dB}} \) will be easily observed. However, if the phase noise is measured using a phase-locked loop, the nonlinear transfer function of the phase detector will change the measured \( \omega_{-3\text{dB}} \). A very complete review of these measurement techniques and their properties can be found in [42–48].

19.2.2. Timing Jitter

As mentioned earlier, uncertainties in the transition instants of a periodic waveform are known as clock jitter. For a free-running oscillator, it increases with the measurement interval \( \tau \) (i.e. the time delay between the reference and the observed transitions). This increase is illustrated in the plot of timing variance shown in Figure 19.8 [32].

This growth in variance, that is, “jitter accumulation”, occurs because any uncertainty in an earlier transition affects all the following transitions, and its effect persists indefinitely. Therefore, the timing uncertainty when \( \tau \) seconds have elapsed includes the accumulative effect of the uncertainties associated with the transitions.

A log–log plot of the timing jitter, \( \sigma_{\tau} \), versus the measurement delay, \( \tau \), for a free-running oscillator will typically exhibit regions with slopes of \( \frac{1}{2} \) and 1 as shown in Figure 19.9. In the region with the slope of \( \frac{1}{2} \), the standard deviation

![Figure 19.8. Clock jitter increasing with distance from the reference edge.](image-url)
of the jitter after \( \tau \) seconds is [32]

\[
\sigma_\tau = \kappa \sqrt{\tau} \quad (19.3)
\]

where \( \kappa \) is a proportionality constant determined by circuit parameters. In a similar fashion, the standard deviation of the jitter in the region with the slope of 1 may be expressed as

\[
\sigma_\tau = \zeta \cdot \tau \quad (19.4)
\]

where \( \zeta \) is another proportionality constant.

In most digital applications, it is desirable for \( \sigma_\tau \) to decrease at the same rate as the frequency increases, to keep constant the ratio of the rms timing jitter to the period. Therefore, phase jitter, defined as

\[
\sigma_{\Delta \phi} = 2\pi \frac{\sigma_\tau}{T} = \omega_0 \sigma_\tau \quad (19.5)
\]

is a more useful measure in many applications. In (19.5), \( T \) is the period of oscillation.

**19.3. Phase Noise Modeling**

We now give a brief introduction to the time-variant phase noise model [27, 33]. In an oscillator, each perturbation source affects both amplitude and phase of the output signal as shown by the variations in excess phase, \( \phi(t) \), and amplitude, \( A(t) \), defined by (19.1). Hence, an equivalent system for phase, can be defined, whose input is a perturbation current (or voltage) and its output is the excess phase, \( \phi(t) \), as shown in Figure 19.10. Figure 19.11 shows the simplified model of a parallel LC tank oscillating with voltage amplitude, \( V_{\text{max}} \).
A current impulse at the input only affects the voltage across the capacitor with no effect on the current through the inductor. This in turn results in an instantaneous change in the tank voltage and hence a shift in the amplitude and phase depending on the time of injection. For a linear capacitor, the instantaneous voltage change $\Delta V$ is given by

$$\Delta V = \frac{\Delta q}{C_{\text{total}}} \quad (19.6)$$

where $\Delta q$ is the total charge injected by the current impulse and $C_{\text{total}}$ is the total capacitance in parallel with the current source. The resultant change in $A(t)$ and $\phi(t)$ is time dependent, as depicted in Figure 19.11. In particular, if the impulse is applied at the peak of the voltage across the capacitor, there will be no phase shift and only an instantaneous amplitude change will result. On the other hand, if this impulse is applied at the zero crossing, it has the maximum effect on the excess phase, $\phi(t)$, and the minimum effect on the amplitude.

There is an important difference between the phase and amplitude responses of practical oscillators. In response to a current impulse, the excess amplitude
undergoes some transient behavior but finally converges to zero because the nonlinear amplitude restoring mechanism existing in any practical oscillator will restore the amplitude to its steady-state value. On the other hand, fluctuations in the excess phase are not quenched by any restoring force and therefore persist indefinitely.

Based on the foregoing argument, a current impulse injecting charge at \( t = \tau \) results in a step change in phase, as shown in Figure 19.11. The height of this step will depend on the instant of charge injection. It is important to note that regardless of the size of the injected charge, the equivalent systems of Figure 19.10 remain time-variant. The injected charge induces a voltage change, \( \Delta V \), which corresponds to a phase shift, \( \Delta \phi \), as shown in the figure. For small injected charge (small area of the current impulse), the resultant phase shift is proportional to the voltage change, \( \Delta V \), and hence to the injected charge, \( \Delta q \). Therefore, \( \Delta \phi \) can be written as

\[
\Delta \phi = \Gamma(\omega_0 \tau) \frac{\Delta V}{V_{\text{max}}} = \Gamma(\omega_0 \tau) \frac{\Delta q}{q_{\text{max}}} \quad \Delta q \ll q_{\text{max}}
\]

where \( V_{\text{max}} \) is the voltage swing across the capacitor and \( q_{\text{max}} = C_{\text{node}} V_{\text{max}} \) is the maximum charge swing. The function, \( \Gamma(x) \), is the time-varying, dimensionless, frequency and amplitude-independent “proportionality factor”. It is called the ISF [27], since it determines the sensitivity of the oscillator to an impulsive input. It describes the amount of excess phase shift resulting from application of a unit impulse at any point in time. Figure 19.12 shows the ISF for an LC and a ring oscillator. The ISF for an LC oscillator with a cosine waveform is approximately a sine function. For the ring oscillator, the ISF is maximum during transitions and minimum during the times that the stage of interest is saturated [33].

The current-to-phase transfer function is linear for small injected charge, even though the active elements may have strongly nonlinear voltage–current behavior. The linearity of the current-to-phase system of Figure 19.10 does

![Figure 19.12. Typical ISF for (a) LC and (b) ring oscillators.](image)
not imply linearization of the nonlinearity of the voltage–current characteristics of the active devices. In fact, this nonlinearity affects the shape of the ISF and, therefore, has an important influence on phase noise. Thus, as long as the injected charge is small, the equivalent systems for phase and amplitude can be fully characterized using their linear time-variant unit impulse responses, $h_{\phi}(t, \tau)$ and $h_{A}(t, \tau)$. Noting that the introduced phase shift persists indefinitely, the unity phase impulse response can be easily written as:

$$h_{\phi}(t, \tau) = \frac{\Gamma(\omega_0 \tau)}{q_{\text{max}}} u(t - \tau)$$  \hspace{1cm} (19.8)

where $u(t)$ is the unit step. For small arbitrary perturbation current injection, $i(t)$, the output excess phase, $\phi(t)$, can be calculated using the superposition integral, that is,

$$\phi(t) = \int_{-\infty}^{\infty} h_{\phi}(t, \tau) i(\tau) \, d\tau = \int_{-\infty}^{t} \frac{\Gamma(\omega_0 \tau)}{q_{\text{max}}} i(\tau) \, d\tau$$  \hspace{1cm} (19.9)

Since the ISF is periodic, it can be expanded in a Fourier series:

$$\Gamma(\omega_0 \tau) = c_0 + \sum_{n=1}^{\infty} c_n \cos(n \omega_0 \tau + \theta_n)$$  \hspace{1cm} (19.10)

where the coefficients $c_n$ are real-valued, and $\theta_n$ is the phase of the $n$th harmonic. As will be seen later, $\theta_n$ is not important for random input noise and is thus neglected here. Using this expansion in the superposition integral and exchanging the order of summation and integration, individual contributions to the total $\phi(t)$ for an arbitrary input current, $i(t)$, injected into any circuit node can be identified in terms of the various Fourier coefficients of the ISF. This decomposition can be better seen with the equivalent block diagram shown in Figure 19.13. Each branch of the equivalent system in this figure acts as a bandpass filter and a down-converter in the vicinity of an integer multiple of the oscillation frequency. For example, the second branch weights the input by $c_1$, multiplies it with a tone at $\omega_0$ and integrates the product. Hence, it passes the frequency components around $\omega_0$ and down-converts the output to the baseband. As can be seen, components of perturbations in the vicinity of integer multiples of the oscillation frequency play the most important role in determining $\phi(t)$. The output voltage, $V(t)$, is related to the phase, $\phi(t)$, through a phase modulation (PM) process as shown in Figure 19.13. The complete process thus can be viewed as a cascade of multiple parallel LTV system that converts current (or voltage) to phase, with a nonlinear system that converts phase to voltage. The evolution of device noise into phase noise due to this process is visualized in Figure 19.14 [27].
Consider a random noise current source, $i_n(t)$, whose power spectral density has both a flat region and a $1/f$ region, as shown in Figure 19.14. Noise components located near integer multiples of the oscillation frequency are weighted by Fourier coefficients of the ISF and integrated to form the low-frequency noise sidebands for $S_\phi(\omega)$. These sidebands in turn become close-in phase noise in the spectrum of $S_\nu(\omega)$ through PM. The total $S_\phi(\omega)$ is given by the sum of phase noise contributions from device noise in the vicinity of the integer multiples of $\omega_0$, weighted by the coefficients $c_n$. This is shown in Figure 19.15, which shows the spectrum of $\phi(t)$ on log–log scales.

The theory predicts the existence of $1/f^3$ and $1/f^2$ regions in the phase noise power spectrum as well as a flat noise floor due to the device amplification noise as shown in Figure 19.15. Low-frequency noise, such as flicker noise, is weighted by the coefficient $c_0$ and ultimately produces a $1/f^3$ phase noise.
White noise terms are weighted by the rms value of the ISF (usually dominated by $c_0$) and give rise to the $1/f^2$ region of phase noise spectrum. The total sideband noise power in the $1/f^2$ region is the sum of the individual terms, as shown by the bold line in the same figure and will be given by [27]:

$$\mathcal{L}(\Delta \omega) = 10 \log \left[ \frac{\Gamma_{\text{rms}}^2}{q_{\text{max}}^2} \cdot \frac{\overline{q}^2}{2 \cdot \Delta \omega^2} \right]$$  \hspace{1cm} (19.11)

### 19.3.1. Up-Conversion of $1/f$ Noise

Many active devices exhibit low-frequency noise with a power spectrum that is approximately inversely proportional to the frequency, usually referred to as $1/f$ noise. It is important to note that nothing in the foregoing development implies that the $1/f^3$ corner of the phase noise and the $1/f$ corner of the device noise are the same. In fact, from Figure 19.15, it should be apparent that the relationship between these two corner frequencies depends on the specific values of $c_0$ and $\Gamma_{\text{rms}}$. The $1/f^3$ corner of phase noise, $\Delta \omega_{1/f^3}$, is smaller than the device $1/f$ noise corner, $\omega_{1/f}$, by a factor determined by the ratio of the dc to rms value of the ISF [27], that is,

$$\Delta \omega_{1/f^3} = \omega_{1/f} \cdot \left( \frac{c_0}{\Gamma_{\text{rms}}} \right)^2$$  \hspace{1cm} (19.12)

The dc value of the ISF is directly affected by certain symmetry properties of the waveform, such as rise and fall time symmetry [27,33,39]. Exploiting these symmetry properties, oscillators with smaller $c_0$ can be designed to minimize
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the up-conversion of $1/f$ noise. Recognizing this fact allows us to identify the design parameters that minimize the up-conversion of low-frequency noise, through proper device sizing, for example.

Symmetry is important to minimize the effect of low-frequency noise, particularly when using surface devices such as MOSFETs. This extra degree of freedom can be exploited to suppress the effect of low-frequency noise on the oscillator phase noise. To understand what affects $e_0$, consider two ring oscillators, with waveforms shown in Figure 19.16. The first waveform has symmetric rising and falling edges, that is, its rise-time is the same as its fall-time. The sensitivity of this oscillator to a perturbation during the rising edge is the same as its sensitivity during the falling edge, except for a sign. Therefore, the ISF has a small dc value. The second case corresponds to an asymmetric waveform with slow rising edge and a fast falling edge. In this case, the phase is more sensitive during the rising edge, and is also sensitive for a longer time; therefore, the positive lobe of the ISF will be taller and wider as opposed to its negative lobe which is short and thinner, as shown in Figure 19.16. It can be shown through simulations and experimentally that the waveform of Figure 19.16(b) results in a larger low-frequency noise up-conversion [27,33].

**19.3.2. Time-Varying Noise Sources**

The time-varying noise sources have an extremely important impact on the phase noise of an oscillator and can be properly modeled using the time-varying approach. In practical oscillators, the statistical properties of some of the random noise sources change with time in a periodic manner. These sources are referred to as cyclostationary. For instance, the channel noise of a MOS transistor in an oscillator is cyclostationary because the periodically time-varying gate–source overdrive modulates the drain noise power. As an example, consider the Colpitts oscillator of Figure 19.17(a). The simulated drain voltage and current of the transistor are shown in Figure 19.17(b). Note that the drain
current consists of a short period of large current followed by a quiet interval [52]. Instantaneous drain current of the transistor controls channel thermal noise power density; therefore, it is the largest during the peak of drain current. Figure 19.17 also shows a sample of drain current noise. The cyclostationary noise current $i_n(t)$ is decomposed as $i_n(t) = i_{n0}(t) \cdot \alpha(\omega_0 t)$, where $i_{n0}(t)$ is a white stationary process and $\alpha(\omega_0 t)$ is a deterministic periodic function describing the noise amplitude modulation and, therefore, is referred to as the noise modulating function (NMF). The cyclostationary noise can be treated as a stationary noise applied to a system with a new ISF given by

$$\Gamma_{\text{eff}}(x) = \Gamma(x) \cdot \alpha(x) \tag{19.13}$$

where $\alpha(\omega_0 t)$ can be derived easily from device noise characteristics and the noiseless steady-state waveform. Note that there is a strong correlation between the cyclostationary noise source and the waveform of the oscillator. The maximum of the noise power always recurs at a certain point of the oscillatory waveform, thus the average of the noise may not be a good representation of the noise power.

The relative timing of the NMF with respect to the ISF can drastically change the effect of those noise sources. For the Colpitts oscillator of Figure 19.17, the surge of drain current occurs at the minimum of the voltage across the tank, where the ISF is small. The channel noise reaches its maximum power for maximum drain current. This lowers the phase noise degradation due to the channel noise, because the maximum noise power always coincides with the minimum phase noise sensitivity. This concept can be more accurately described using the rms value of the effective ISF. Functions $\Gamma(x)$, $\alpha(x)$ and $\Gamma_{\text{eff}}(x)$ for this oscillator are shown in Figure 19.18. Note that, in this case, $\Gamma_{\text{eff}}(x)$ has a much smaller rms value than $\Gamma(x)$, and hence the effect of cyclostationarity is very significant for the LC oscillator and cannot be neglected.
19.4. Phase Noise Trade-Offs in LC Oscillators

Due to their relatively good phase noise, ease of implementation and differential operation, LC oscillators play an important role in high-frequency circuit design [35–41]. We now present design implications in single-ended and differential oscillators.

19.4.1. Tank Voltage Amplitude

Tank voltage amplitude has an important effect on the phase noise, as emphasized by the presence of $q_{\max}$ in the denominator of (19.11). In this subsection, we will derive expressions for the tank amplitude of different types of LC oscillators. The effect of the nonlinearity on the oscillator amplitude can be evaluated using describing function analysis [49–54].

Consider the forward path transconductance block, $G$, in the two-port model of Figure 19.19(a). It will be assumed that it comprises a memoryless nonlinearity as shown in Figure 19.19(b). In an oscillator with a reasonably high tank $Q$, the output voltage of the frequency selective network of Figure 19.19 will be very close to a sinusoidal voltage even for a periodic non-sinusoidal input current, as shown in Figure 19.20.

Since the output voltage of the frequency selective network is the input to the nonlinear transconductance block, the response of the nonlinear block, $G$, to a sinusoidal input should be characterized. Although the output current of the nonlinear transconductance will not be sinusoidal, the frequency selective network will mainly pass the fundamental term of the input since it will attenuate all the other harmonics significantly. Therefore, it is the gain from the...
input sinusoidal voltage to the fundamental component of the output current that determines the loop gain.

Based on the foregoing observations, the nonlinear transconductance is assumed to be driven with a sinusoidal input of amplitude $V_1$. In the most general case, the output will have all the terms of the Fourier series. Thus, for an input voltage of the following form:

$$v_{in}(t) = V_1 \cos(\omega_0 t)$$  \hspace{1cm} (19.14)

the output current can be written as

$$i_{out}(t) = \sum_{n=1}^{\infty} I_n \cos(n\omega_0 t)$$  \hspace{1cm} (19.15)

The amplitude ratio of the fundamental output component to the input is the magnitude of the describing function, which will be denoted as $G_m(V_1)$, or $G_m$ for short. Thus,

$$G_m(V_1) = \frac{I_1}{V_1}$$  \hspace{1cm} (19.16)

This naming convention underscores that $G_m$ is the effective large signal transconductance of the nonlinear block at $\omega_0$.

Although it is possible to derive the large signal transconductance, $G_m$, for various active devices [52], investigating the two extreme cases of very large
and very small values of $V_1$ provides important information. For very small-values of $V_1$, the small-signal assumption holds and the output grows linearly with input. Therefore,

$$G_m(V_1) = g_m = \frac{I_{\text{tail}}}{V_T} \quad V_1 \ll V_T$$

(19.17)

where $g_m$ is the small-signal transconductance of the transistor.

For large input amplitude, the output current will consist of sharp spikes of current, whose average value necessarily equals $I_{\text{bias}}$. Therefore, the fundamental component of the output current can be approximated by

$$I_1 = \frac{2}{T} \int_0^T i(t) \cos(\omega_0 t) \, dt \approx \frac{2}{T} \int_0^T i(t) \, dt = 2I_{\text{bias}}$$

(19.18)

where $T$ is the period of the oscillation. For large values of $V_1$, the spikes will be very thin and tall and will occur at the peak of the cosine function. This approximation holds as long as the spikes are sharp enough so that the cosine can be approximated as one for the duration of the spike. Hence, the describing function for large values of $V_1$ can be written as

$$G_m(V_1) = \frac{2I_{\text{tail}}}{V_1} \quad V_1 \gg V_T$$

(19.19)

As can be seen, the large signal transconductance is inversely proportional to the input voltage amplitude for large values of input voltage. This inverse proportionality provides a negative feedback mechanism that stabilizes the amplitude of oscillations by reducing the effective gain as the amplitude grows.

It is noteworthy that (19.19) is valid for other types of devices with monotonic nonlinearity, such as MOS transistors, vacuum tubes, etc., as long as $V_1$ is larger than a characteristic voltage that depends on the particular device of interest. This universality holds because the only assumption used to obtain (19.19) is that the spikes are so thin that the cosine function can be approximated as one for the duration of the spike.

Describing function analysis can be applied to calculate the amplitude and frequency of oscillation. As an example, consider the common gate MOS Colpitts oscillator of Figure 19.17. The large signal equivalent circuit for the oscillator of Figure 19.17 can be shown as in Figure 19.21. The tank voltage amplitude is related to $V_1$ through

$$V_1 = V_{\text{tank}} \frac{C_1}{C_1 + C_2} = nV_{\text{tank}}$$

(19.20)

where

$$n = \frac{C_1}{C_1 + C_2}$$

(19.21)
is the capacitive voltage division ratio. In steady state, tank current is related to the tank voltage through

\[ I_{\text{tank}} = Y_{\text{tank}} V_{\text{tank}} = \left( n^2 G_m + G_L + jC_{eq}\omega + \frac{1}{jL\omega} \right) V_{\text{tank}} = nG_m V_{\text{tank}} \]  

(19.22)

where \( Y_{\text{tank}} \) and \( G_L \) are the admittance and effective parallel conductance of the tank, respectively. For (19.22) to hold, we should have

\[ \omega_0 = \frac{1}{\sqrt{LC}} \]  

(19.23)

and

\[ G_L = n(1 - n)G_m \]  

(19.24)

Using (19.19) and (19.20), the tank voltage amplitude is calculated to be

\[ V_{\text{tank}} = 2R_L I_{\text{tail}} (1 - n) \]  

(19.25)

As can be seen from (19.25), for small \( C_1/C_2 \) ratios, the tank voltage amplitude is about twice the product of tail current and effective tank resistance. This mode of operation is usually referred to as current limited.

Note that (19.25) breaks down for small values of \( I_{\text{tail}} \) in accordance with (19.17). It also fails for large values of \( I_{\text{tail}} \) as \( V_{\text{tank}} \) approaches \( V_{\text{DD}} \). This failure happens as the MOS transistor enters the ohmic region (or saturation for a bipolar transistor) for part of the period, therefore violating the assumptions leading to (19.25). The value of \( V_{\text{tank}} \) for which this happens depends on the supply voltage, and therefore this regime of operation is known as voltage limited.

A simple expression for the tank amplitude of the differential complementary CMOS LC oscillator of Figure 19.22 can be obtained by assuming that the differential stage switches quickly from one side to another. Figure 19.22 shows
the current flowing in the complementary cross-coupled differential LC oscillator [36,39] when it is completely switched to one side. As the tank voltage changes, the direction of the current flow through the tank reverses. The differential pair thus can be modeled as a current source switching between $I_{\text{tail}}$ and $-I_{\text{tail}}$ in parallel with an RLC tank, as shown in Figure 19.23. $R_{\text{eq}}$ is the equivalent parallel resistance of the tank.

At the frequency of resonance, the admittances of the $L$ and $C$ cancel, leaving $R_{\text{eq}}$. Harmonics of the input current are strongly attenuated by the $LC$ tank, leaving the fundamental of the input current to induce a differential voltage swing of amplitude $(4/\pi)I_{\text{tail}}R_{\text{eq}}$ across the tank if one assumes a rectangular current waveform. At high frequencies, the current waveform may be approximated more closely by a sinusoid due to finite switching time and limited gain. In such cases, the tank amplitude can be better approximated as

$$V_{\text{tank}} \approx I_{\text{tail}}R_{\text{eq}}$$  \hspace{1cm} (19.26)

This current-limited regime of operation since in this regime, the tank amplitude is solely determined by the tail current source and the tank equivalent resistance. Note that (19.26) loses its validity as the amplitude approaches the supply voltage because both NMOS and PMOS pairs will enter the triode region at the
peaks of the voltage and the oscillator will operate in the voltage-limited regime. Also, the tail NMOS transistor may spend most (or even all) of its time in the linear region. The tank voltage will be clipped at $V_{DD}$ by the PMOS transistors and at ground by the NMOS transistors, and hence cannot significantly exceed $V_{DD}$. Note that since the tail transistor is in the triode region, the current through the differential NMOS transistors can drop significantly when their drain–source voltage becomes very small.

Figure 19.24 shows the simulated tank voltage amplitude as a function of tail current for three different values of $V_{DD}$. As can be seen, the tank amplitude is proportional to the tail current in the current-limited region, while it is limited by $V_{DD}$ in the voltage-limited regime.

### 19.4.2. Noise Sources

In general, noise sources in an oscillator are cyclostationary because of the periodic changes in currents and voltages of the active devices. In this subsection, the noise sources in the cross-coupled LC oscillator of Figure 19.22 and the single-ended Colpitts oscillator of Figure 19.17 will be examined.

**Stationary noise approximation.** Figure 19.25 depicts the noise sources in the complementary differential LC oscillator. The noise power densities for these sources are required to calculate the phase noise. In a simplified stationary approach, the power densities of the noise sources can be evaluated at the most sensitive time (i.e. the zero-crossing of the differential tank voltage) to estimate the effect of these sources. Figure 19.26(a) shows a simplified model of the sources in this balanced case for the differential LC oscillator. Converting the current sources to their Thévenin equivalent and writing KVL,
Trade-Offs in Oscillator Phase Noise

one obtains the equivalent differential circuit shown in Figure 19.26(b). Note that the parallel resistance is canceled by the negative resistance provided by the positive feedback. Therefore, the total differential noise power due to the four cross-coupled transistors is

\[
\bar{i}_{cc}^2 = \frac{1}{4} \left( \bar{i}_{n1}^2 + \bar{i}_{n2}^2 + \bar{i}_{p1}^2 + \bar{i}_{p2}^2 \right) = \frac{1}{2} \left( \bar{i}_{n}^2 + \bar{i}_{p}^2 \right) \tag{19.27}
\]

where \(\bar{i}_{n}^2 = \bar{i}_{n1}^2 = \bar{i}_{n2}^2\) and \(\bar{i}_{p}^2 = \bar{i}_{p1}^2 = \bar{i}_{p2}^2\). Noise densities \(\bar{i}_{n}^2/\Delta f\) and \(\bar{i}_{p}^2/\Delta f\) are given by [55]

\[
\bar{i}_{n}^2/\Delta f = 4kT\mu C_{ox} \frac{W}{L} (V_{GS} - V_T) \tag{19.28}
\]

where \(\mu\) is the mobility of the carriers in the channel, \(C_{ox}\) is the oxide capacitance per unit area, \(W\) and \(L\) are the width and length of the MOS transistor,
respectively, $V_{GS}$ is the dc gate-source voltage and $V_T$ is the threshold voltage. Equation (19.28) is valid for both short and long-channel regimes of operation. However $\gamma$ is around $2/3$ for long-channel transistors while it may be between 2 and 3 in the short-channel region [56].

In addition to these sources, the contribution of the effective series resistance of the inductor, $r_s$, caused by ohmic losses in the metal and substrate is given by

$$\frac{i_{rs}^2}{\Delta f} = 4kT \frac{r_s C}{L} = \frac{4kT}{R_p}$$

where $R_p \approx Q^2 r_s = (L \omega_0)^2 / r_s$ is the equivalent parallel resistance at the frequency of oscillation.

**Cyclostationary noise sources.** To investigate the effect of cyclostationary noise source and see the effect of fast switching in the transistors, the single-ended Colpitts oscillator of Figure 19.17 was simulated for various channel mobilities, while keeping other parameters constant. The higher mobility results in larger transconductance and hence a faster switching time, without affecting the tank amplitude significantly. The amplitude remains constant as in the current-limited regime, the tail current and tank loss determine the amplitude according to (19.25). The simulated NMF and the effective ISFs for various values of mobility are shown in Figure 19.27. The drain voltage and the oscillation frequency do not change significantly, as predicted by (19.25) and hence the ISF does not change.

![Figure 19.27](image)
Trade-Offs in Oscillator Phase Noise

Note that the lobes of the effective ISF, $\Gamma_{eff}(x)$ become shorter and thinner for larger mobility (or equivalently for higher transconductance per current). The fast switching of the transistors is essential to achieve current pulses as sharp as possible, and hence transistors with lowest parasitic capacitance per maximum deliverable current are highly desirable. This will in turn result in a much lower channel noise contribution. The simulated phase noise improvements for the Colpitts oscillator of Figure 19.17, are summarized in Table 19.1. The improvements are measured in reference to the stationary noise source due to the same bias current. As can be seen, significant improvements in the phase noise can be achieved using devices with higher mobility. This suggests that a class C operation is desirable for the oscillator to achieve the best phase noise performance. Phase noise improvement for different channel mobilities due to cyclostationary noise alignment.

<table>
<thead>
<tr>
<th>$\mu$ (cm$^2$/Vs)</th>
<th>Phase noise improvement (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>250</td>
<td>0.4</td>
</tr>
<tr>
<td>350</td>
<td>3.5</td>
</tr>
<tr>
<td>1000</td>
<td>6.7</td>
</tr>
<tr>
<td>2000</td>
<td>9.2</td>
</tr>
</tbody>
</table>

Note that the lobes of the effective ISF, $\Gamma_{eff}(x)$ become shorter and thinner for larger mobility (or equivalently for higher transconductance per current). The fast switching of the transistors is essential to achieve current pulses as sharp as possible, and hence transistors with lowest parasitic capacitance per maximum deliverable current are highly desirable. This will in turn result in a much lower channel noise contribution. The simulated phase noise improvements for the Colpitts oscillator of Figure 19.17, are summarized in Table 19.1. The improvements are measured in reference to the stationary noise source due to the same bias current. As can be seen, significant improvements in the phase noise can be achieved using devices with higher mobility. This suggests that a class C operation is desirable for the oscillator to achieve the best phase noise performance. Phase noise improvement for different channel mobilities due to cyclostationary noise alignment.

19.4.3. Design Implications

To gain more insight about the trade-offs involved, the complimentary differential LC VCO of Figure 19.22 was fabricated. The phase noise at 600 kHz offset is measured for different values of the tail current, as shown in Figure 19.28. As can be seen from this graph, increasing the tail current will improve the phase noise due to the increase in oscillation amplitude. Also, the improvement slows down as the tank voltage amplitude approaches the supply voltage. It can also be shown [39] that the phase noise has a weak dependence on the supply voltage, improving somewhat for lower voltages. This behavior may be attributed to smaller voltage drops across the channel on the MOS transistors which reduces the effect of velocity saturation in the short-channel regime and hence lowers $\gamma$.

The power dissipation increases as the operation point moves toward higher tail currents and supply voltage. If the design goal is to achieve the minimum phase noise without any concern for power dissipation, the oscillator should be operated at high supply voltage and high current to allow the maximum possible tank voltage amplitude. However, power usually is a concern, so a
more practical goal maybe to achieve the best phase noise for a given power. Equation (19.11) suggests that it is desirable to operate at the largest tank amplitude for a given power dissipation. However, the tank amplitude cannot be increased beyond $V_{DD}$ due to voltage limiting. Therefore, according to this simple model, it is desirable to operate at the edge of the voltage-limited mode of operation.

19.5. Phase Noise Trade-Offs for Ring Oscillators

Due to the ease of integration and large tuning range, ring oscillators have become an essential building block in many digital and communication systems. In this section, we will derive closed-form expressions for the rms and dc values of the ISF for ring oscillators. These approximate rms and dc values are used to obtain closed-form expressions for phase noise and jitter in ring oscillators. Finally, design trade-offs such as the question of single-ended vs differential implementation of ring oscillators and the optimum number of stages are addressed.

19.5.1. The Impulse Sensitivity Function for Ring Oscillators

To calculate phase noise and jitter using (19.11) and (19.12), one needs to know the dc and rms values of the ISF. In this subsection, approximate closed-form equations for the dc and rms values of the ISF of ring oscillators will be obtained.
It is instructive to look at the actual ISF of ring oscillators to gain insight into what constitutes a good approximation. Figure 19.29 shows the shape of the ISF for a group of single-ended CMOS ring oscillators. The frequency of oscillation is kept constant (through adjustment of channel length), while the number of stages is varied from 3 to 15 (in odd numbers). The ISF is calculated by injecting very short pulses of current and measuring the resultant phase shift.

As can be seen, increasing the number of stages reduces the peak value of the ISF. The reason is that the transitions of the normalized waveform become faster for larger $N$ in this constant frequency scenario. Since the sensitivity is inversely proportional to the slope, the peak of the ISF drops. Also, the widths of the lobes of the ISF decrease as $N$ becomes larger since each transition occupies a smaller fraction of the period. Based on these observations, the ISF of ring oscillators with equal rise and fall times can be approximated as two identical triangles, as shown in Figure 19.30.

The ISF has a maximum of $1/f_{\text{max}}'$, where $f_{\text{max}}'$ is the maximum slope of the normalized waveform $f$ in (19.1). Also, the width of the triangles is approximately $2/f_{\text{max}}'$ and hence the slopes of the sides of the triangles are $\pm 1$. Therefore, assuming equality of the rise and fall times, $\Gamma_{\text{rms}}$ can be estimated as

$$\Gamma_{\text{rms}}^2 = \frac{1}{2\pi} \int_0^{2\pi} \Gamma^2(x) \, dx = \frac{4}{2\pi} \int_0^{1/f_{\text{max}}'} x^2 \, dx = \frac{2}{3\pi} \left( \frac{1}{f_{\text{max}}'} \right)^3$$  \hspace{1cm} (19.30)

On the other hand, stage delay is proportional to the rise-time:

$$\hat{t}_D = \frac{\eta}{f_{\text{max}}'}$$  \hspace{1cm} (19.31)
where $\hat{f}_D$ is the stage delay normalized to the period and $\eta$ is a proportionality constant, which is typically close to one, as can be seen in Figure 19.31.

The period is $2N$ times longer than a single stage delay, that is,

$$2\pi = 2N\hat{f}_D = \frac{2N\eta}{f'_{\max}} \quad (19.32)$$

Using (19.30) and (19.32), the following approximate expression for $\Gamma_{\text{rms}}$ is obtained:

$$\Gamma_{\text{rms}} \approx \sqrt{\frac{2\pi^2}{3\eta^3}} \cdot \frac{1}{N^{1.5}} \quad (19.33)$$

Note that the $1/N^{1.5}$ dependence of $\Gamma_{\text{rms}}$ is independent of the value of $\eta$. Figure 19.32 illustrates $\Gamma_{\text{rms}}$ vs the number of stages for the ISFs shown in
Figure 19.29 with plus signs on log–log axes. The solid line shows the line of $\Gamma_{\text{rms}} \approx 4/N^{1.5}$, which is obtained from (19.33) for $\eta = 0.75$. To verify the generality of (19.33), a second set of simulations was performed in which a fixed channel length is maintained for all the devices in the inverters while varying the number of stages to allow different frequencies of oscillation. Again $\Gamma(x)$ is directly simulated and its rms value is plotted in Figure 19.32 with circles. This simulation is repeated with a different supply voltage (3 V as opposed to 5 V) and the result is shown with crosses. As can be seen, the values of $\Gamma_{\text{rms}}$ are almost identical for these three cases.

It should not be surprising that $\Gamma_{\text{rms}}$ is primarily a function of $N$ because the effect of variations in other parameters, such as $q_{\text{max}}$ and device noise, have already been decoupled from $\Gamma(x)$; the ISF is a unitless, frequency and amplitude independent function.

Equation (19.33) is valid for differential ring oscillators as well, since in its derivation no assumption specific to single-ended oscillators was made. Figure 19.33 shows $\Gamma_{\text{rms}}$ for three sets of differential ring oscillators, with a varying number of stages (4–16). The data shown with plus signs correspond to oscillators in which the total power dissipation and drain voltage swing are kept constant by scaling the tail current sources and load resistors as $N$ changes. Members of the second set of oscillators have a fixed total power dissipation and fixed load resistors, which result in variable swings, and for whom data are shown with circles. The third case is that of a fixed tail current for each stage and constant load resistors, whose data are illustrated using crosses. Again,
despite the diverse variations of frequency and other circuit parameters, the 
\(1/N^{1.5}\) dependency of \(\Gamma_{\text{rms}}\) and its independence from other circuit parameters
still holds. In the case of a differential ring oscillator, \(\Gamma_{\text{rms}} \approx 3/N^{1.5}\), which corresponds to \(\eta = 0.9\), is the best fit approximation for \(\Gamma_{\text{rms}}\). This is shown with the solid line in Figure 19.33.

Although \(\Gamma_{\text{rms}}\) decreases as the number of stages increases, one should not conclude that the phase noise can be reduced using a larger number of stages, because the number of noise sources, as well as their magnitudes, also increases, for a given total power dissipation and frequency of oscillation. The question of optimal number of stages is, therefore, a bit involved, and will be addressed in the subsequent sections.

In the case of unequal rise and fall times, a similar approximation can be used to calculated the dc and rms value of the ISF and hence relating the \(1/f^3\) phase noise corner to the device \(1/f\) noise corner through [33]

\[
f_{1/f^3} = f_{1/f} \cdot \frac{3}{2\eta N} \cdot \frac{(1 - A)^2}{1 - A + A^2}
\]

(19.34)

where \(A\) represents the asymmetry of the waveform and is defined as

\[
A \equiv \frac{f'_{\text{rise}}}{f'_{\text{fall}}}
\]

(19.35)

where \(f'_{\text{rise}}\) and \(f'_{\text{fall}}\) are the maximum slope during the rising and falling edges, respectively.
In the case of asymmetric rising and falling edges, both \( \Gamma_{\text{rms}} \) and \( c_0 \) will change. The \( 1/f^3 \) corner of the phase noise spectrum is inversely proportional to the number of stages. Therefore, the \( 1/f^3 \) corner can be reduced either by making the transitions more symmetric in terms of rise and fall times or by increasing the number of stages. Although the former always helps, the latter has important implications on the phase noise in the \( 1/f^2 \) region, as will be shown later.

### 19.5.2. Expressions for Phase Noise in Ring Oscillators

It is desirable to express phase noise and jitter in terms of design parameters such as power dissipation and frequency to be able to investigate the design trade-offs more readily. Throughout this subsection, we will focus on the white noise as it is assumed that the symmetry criteria for minimizing the up-conversion of \( 1/f \) noise are already met. For CMOS transistors, the drain current noise spectral density is given by (19.28), which is valid in both short and long-channel regimes, as long as an appropriate value for \( \gamma \) is used. The first case considered is a single-ended CMOS ring oscillator with equal-length NMOS and PMOS transistors. Assuming \( V_{\text{TN}} = V_{\text{TP}} \), the maximum total channel noise from the NMOS and PMOS devices, when both the input and output are at \( V_{DD}/2 \), is given by

\[
\frac{i_n^2}{\Delta f} = \left( \frac{i_n^2}{\Delta f} \right)_N + \left( \frac{i_n^2}{\Delta f} \right)_P = 4kT\gamma \mu_{\text{eff}} C_{\text{ox}} \frac{W_{\text{eff}}}{L} \Delta V
\]  

(19.36)

where

\[
W_{\text{eff}} = W_n + W_p
\]  

(19.37)

and

\[
\mu_{\text{eff}} = \frac{\mu_n W_n + \mu_p W_p}{W_n + W_p}
\]  

(19.38)

and \( \Delta V \) is the gate overdrive in the middle of the transition, that is, \( \Delta V = V_{DD}/2 - V_T \).

During one period, each node is charged to \( q_{\text{max}} \) and then discharged to zero. In an \( N \)-stage single-ended ring oscillator, the power dissipation associated with this process is \( N q_{\text{max}} V_{DD} f_0 \). However, during the transitions, some extra current, also known as crowbar current, is drawn from the supply. This current does not contribute to charging and discharging the capacitors since it goes directly from supply to ground through both transistors. These two components of the total current drawn from supply are shown in Figure 19.34. In a symmetric ring oscillator, these two components are comparable and their difference will
depend on the ratio of the rise-time to stage delay; therefore, the total power dissipation is approximately given by

\[ P = 2\eta N V_{DD} q_{\text{max}} f_0 \]  

(19.39)

Assuming \( \mu_n W_n = \mu_p W_p \) to make the waveforms symmetric to first order, the frequency of oscillation for long-channel devices can be approximated by

\[ f_0 = \frac{1}{2N t_D} = \frac{1}{\eta N (t_r + t_f)} \approx \frac{\mu_{\text{eff}} W_{\text{eff}} C_{\text{ox}} \Delta V^2}{8\eta N L q_{\text{max}}} \]  

(19.40)

where \( t_D \) is the delay of each stage and \( t_r \) and \( t_f \) are the rise and fall-time associated with the maximum slope during a transition.

Assuming that the thermal noise sources of the different devices are uncorrelated, and assuming that the waveform (and hence the ISF) of all the nodes are the same except for a phase shift, the total phase noise due to all \( N \) noise sources is \( N \) times the value given by (19.11). Taking only these inevitable noise sources into account, (19.11), (19.33), (19.36), (19.39) and (19.40) result in the following expression for phase noise:

\[ \mathcal{L}(\Delta \omega) \approx \frac{8}{3\eta} \frac{kT}{P} \cdot \frac{V_{DD}}{V_{\text{char}}} \cdot \frac{\omega_0^2}{\Delta \omega^2} \]  

(19.41)

where \( V_{\text{char}} \) is the characteristic voltage of the device. For long-channel devices, \( V_{\text{char}} = \Delta V / \gamma = (V_{GS} - V_T) / \gamma \). Any extra disturbance, such as substrate and supply noise, or noise contributed by extra circuitry or asymmetry in the waveform, will result in a larger number than (19.41). As can be seen, the phase noise is inversely proportional to the power dissipation and grows quadratically with the oscillation frequency. Further, note the lack of dependence on the number of stages (for a given power dissipation and oscillation frequency). Evidently, the increase in the number of noise sources (and in the maximum power due to the higher transition currents required to run at the same frequency) essentially cancels the effect of decreasing \( \Gamma_{\text{rms}} \).
as \( N \) increases, leading to no net dependence of phase noise on \( N \). Also in using (19.41), one should verify the validity of the assumptions leading to this expression. To calculate the phase noise of an arbitrary oscillator, (19.11) should be used.

A similar calculation for the short-channel case can be carried out. For such devices, phase noise will be still given by (19.41), except for a new \( V_{\text{char}} \):

\[
V_{\text{char}} = \frac{E_c L}{\gamma} \tag{19.42}
\]

which results in a larger phase noise than the long-channel case by a factor of \( \gamma \Delta V / E_c L \). As before, note the lack of dependence on the number of stages in the case of short-channel devices.

Now consider a differential MOS ring oscillator with resistive load. The total power dissipation is

\[
P = NI_{\text{tail}} V_{\text{DD}} \tag{19.43}
\]

where \( N \) is the number of stages, \( I_{\text{tail}} \) is the tail bias current of the differential pair, and \( V_{\text{DD}} \) is the supply voltage. The frequency of oscillation can be approximated by

\[
f_0 = \frac{1}{2Nt_D} \approx \frac{1}{2\eta Nt_I} \approx \frac{I_{\text{tail}}}{2\eta Nq_{\text{max}}} \tag{19.44}
\]

The noise of the tail current source in the vicinity of \( f_0 \) does not affect the phase noise. Rather, its low frequency noise as well as its noise in the vicinity of even multiples of the oscillation frequency affect the phase noise [33,39]. Tail noise in the vicinity of even harmonics can be significantly reduced by a variety of means, such as with a series inductor or a parallel capacitor. As before, the effect of low frequency noise can be minimized by exploiting symmetry. Therefore, only the noise of the differential transistors and the load is taken into account, as shown in Figure 19.35. The total current noise on each single-ended node is given by

\[
\frac{\overline{I_n^2}}{\Delta f} = \left( \frac{\overline{I_n^2}}{\Delta f} \right)_N + \left( \frac{\overline{I_n^2}}{\Delta f} \right)_{\text{load}} = 4kT I_{\text{tail}} \left( \frac{1}{V_{\text{char}}} + \frac{1}{R_L I_{\text{tail}}} \right) \tag{19.45}
\]

where \( R_L \) is the load resistor, \( V_{\text{char}} = (V_{\text{GS}} - V_T) / \gamma \) for a balanced stage in the long-channel limit and \( V_{\text{char}} = E_c L / \gamma \) in the short-channel regime. Assuming zero correlation among the various noise sources, the phase noise due to all \( 2N \) noise sources is \( 2N \) times the value given by (19.11). Using (19.33), the expression for the phase noise of the differential MOS ring oscillator is

\[
L_{\min} \{ \Delta \omega \} \approx \frac{8}{3\eta} \cdot N \cdot \frac{kT}{P} \cdot \left( \frac{V_{\text{DD}}}{V_{\text{char}}} + \frac{V_{\text{DD}}}{R_L I_{\text{tail}}} \right) \cdot \frac{\omega_0^2}{\Delta \omega^2} \tag{19.46}
\]
Chapter 19

The foregoing equations are valid in both long and short-channel regimes of operation with the right choice of $V_{\text{char}}$.

Note that in contrast with the single-ended ring oscillator, a differential oscillator does exhibit a phase noise and jitter dependency on the number of stages, with the phase noise degrading as the number of stages increases for a given frequency and power dissipation. This result may be understood as a consequence of the necessary reduction in charge swing that is required to accommodate a constant frequency of oscillation at a fixed power level as $N$ increases. At the same time, increasing the number of stages at a fixed total power dissipation demands a proportional reduction of tail current sources, which will reduce the swing, and hence $q_{\text{max}}$, by a factor of $1/N^2$.

19.5.3. Substrate and Supply Noise

Noise sources on different nodes of an oscillator may be strongly correlated. This correlation can be due to various reasons. Two examples of sources with strong correlation are substrate and supply noise. These noise sources usually arise from current switching in other parts of the chip. The current fluctuations induce voltage fluctuations across the series resistance and inductance of the bondwires and pins. These fluctuations on the supply and substrate will induce a similar perturbation on different stages of the ring oscillator.

To understand the effect of this correlation, consider the special case of having identical noise sources on all the nodes of the ring oscillator as shown in Figure 19.36. If all the inverters in the oscillator are the same, the ISF for different nodes will differ only in phase by multiples of $2\pi/N$, as shown in Figure 19.37 for $N = 5$. Therefore, the total phase due to all the sources is
determined by superposition, that is,

\[
\phi(t) = \frac{1}{q_{\text{max}}} \sum_{n=0}^{N-1} \int_{-\infty}^{t} i(\tau) \Gamma \left( \omega_0 \tau + \frac{2\pi n}{N} \right) d\tau \\
= \frac{1}{q_{\text{max}}} \int_{-\infty}^{t} i(\tau) \left[ \sum_{n=0}^{N-1} \Gamma \left( \omega_0 \tau + \frac{2\pi n}{N} \right) \right] d\tau
\]  \quad (19.47)

Expanding the term in brackets in a Fourier series, it can be observed that it is zero except at dc and multiples of \(N\omega_0\), that is,

\[
\phi(t) = \frac{N}{q_{\text{max}}} \sum_{n=0}^{\infty} c(nN) \int_{-\infty}^{t} i(\tau) \cos(nN\omega_0 \tau) d\tau \]  \quad (19.48)

which means that for fully correlated sources, only noise in the vicinity of integer multiples of \(N\omega_0\) affects the phase.
19.5.4. Design Trade-Offs in Ring Oscillators

A commonly asked question is the preferred topology for MOS ring oscillators, that is, which one of the single-ended or the differential topologies results in better jitter and phase noise performance for a given center frequency, $f_0$, and total power dissipation, $P$.

Equations (19.41) and (19.46) can be used to compare the phase noise performance of single-ended and differential MOS ring oscillators in the thermal noise limited case. As can be seen for $N$ stages, the phase noise of a properly designed differential ring oscillator is approximately $N[1 + V_{\text{char}}/(R_L I_{\text{tail}})]$ times larger than the phase noise of a single-ended oscillator of equal $N$, $P$ and $f_0$. Since the minimum $N$ for a regular ring oscillator is three, even a properly designed differential CMOS ring oscillator underperforms its single-ended counterpart, with disparity increasing with the large number of stages. This difference is even more pronounced if proper precautions to reduce the noise of the tail current are not taken.

The difference in the behavior of these two types of oscillators with respect to the number of stages can be traced to the way they dissipate power. The dc current drawn from the supply is independent of the number and slope of the transitions in differential ring oscillators. On the contrary, inverter-chain ring oscillators dissipate power mainly on a per transition basis and, therefore, have a better phase noise for a given power dissipation. This difference becomes even larger as the number of stages increases. However, a differential topology may still be preferred in ICs with a large amount of digital circuitry because of the lower sensitivity to substrate and supply noise, as well as lower noise injection into other circuits on the same chip. The decision of which architecture to use should be based on both of these considerations.

Another commonly debated question concerns the optimum number of inverter stages in a ring oscillator to achieve the best jitter and phase noise for a given $f_0$ and $P$. As seen in (19.41), for single-ended oscillators, the phase noise and jitter in $1/f^2$ region are not strong functions of the number of stages for single-ended CMOS ring oscillators. However, if the symmetry criteria are not well satisfied, and/or the process has large $1/f$ noise, (19.34) predicts that a larger $N$ will reduce the phase noise. In general, the choice of the number of stages must be made on the basis of several design criteria, such as $1/f$ noise effect, the desired maximum frequency of oscillation, and the influence of external noise sources, such as supply and substrate noise, that may not scale with $N$.

The phase noise behavior is different for differential ring oscillators. As (19.46) suggests, phase noise increases with an increasing number of stages. Hence, if the $1/f$ noise corner is not large, and/or proper symmetry measures have been taken, the minimum number of stages (3 or 4) should be used to give the best performance. This recommendation holds even if the power dissipation
is not a primary issue. It is not fair to argue that burning more power in a larger number of stages allows the achievement of better phase noise, since dissipating the same total power in a smaller number of stages with larger devices results in better phase noise, as long as it is possible to maximize the total charge swing.

Substrate and supply noise are among other important sources of noise and can be dominant in large digital environments. There are two major differences between these noise sources and internal device noise. First, the power spectral density of these sources is usually non-white and often demonstrates strong peaks at various frequencies [57]. Even more important is that the substrate and supply noise on different nodes of the ring oscillator have a very strong correlation.

A very important insight can be obtained from (19.48). It shows that for the correlated part of the noise, only the \( c_n \) values associated with integer multiples of number of stages, \( N \), contribute to total phase fluctuations. Therefore, every effort should be made to maximize the correlated part of substrate and supply noise. This can be done by making the inverter stages and the noise sources on each node as similar to each other as possible by proper layout and circuit design.

The layout should be kept symmetrical. The inverter stages should be laid out close to each other so that substrate noise appears as a common-mode source. This consideration is particularly important in the case of a lightly doped substrate, since such a substrate may not act as a single node. It is also important that the orientation of all the stages be kept identical. The interconnecting wires between the stages must be identical in length and shape.

The circuit should be designed so that the same supply line goes to all the inverter stages. Also the loading from the stages being driven should be kept identical for all the nodes, for example, by using dummy buffer stages on all the nodes. A larger number of stages will also be helpful because a smaller number of \( c_n \) coefficients will affect the phase noise. Finally, the low-frequency portion of the substrate and supply noise plays an important role in the jitter and phase noise. Fortunately, the effect of low-frequency noise can be reduced by exploiting symmetry to minimize \( c_0 \).

References


